What is claimed is:

1. A method for forming a multi-bit stacked-type non-volatile memory, comprising:

providing a substrate;

forming a patterned dielectric layer containing arsenic on the substrate, wherein the patterned dielectric layer defines a first opening, and the first opening exposes a portion of the substrate and a side wall of the patterned dielectric layer;

forming a dielectric spacer on the side wall of the patterned dielectric layer;

forming a source/drain region in the substrate;

forming a gate dielectric layer on the exposed portion of the substrate;

forming a spacer-shaped floating gate on a side wall of the dielectric spacer and over the gate dielectric layer;

forming an interlayer dielectric layer covering the spacer-shaped floating gate; and

forming a control gate covering the first opening.

2. The method of claim 1, wherein the step of forming the patterned dielectric layer further comprises:

forming a dielectric layer containing arsenic on the substrate;

forming a patterned photoresist layer on the dielectric layer, wherein the patterned photoresist layer defines the first opening;

etching the dielectric layer to form the patterned dielectric layer by using the patterned photoresist layer as a mask, wherein the portion of the substrate and the side wall of the patterned dielectric layer are exposed; and

removing the patterned photoresist layer.

3. The method of claim 1, wherein the step of forming the dielectric spacer further comprises:

forming a conformal dielectric layer covering the substrate; and

anisotropically etching the conformal dielectric layer to form the dielectric spacer on the side wall of the patterned dielectric layer.

4. The method of claim 1, wherein the step of forming the source/drain region further comprises diffusing arsenic atoms of the patterned dielectric layer into the substrate by a thermal driving process.

5. The method of claim 1, wherein the step of forming the gate dielectric layer comprises using thermal oxidation process.

6. The method of claim 1, wherein the step of forming the spacer-shaped floating gate further comprises:

forming a conformal polysilicon layer covering the substrate; and

anisotropically etching the conformal polysilicon layer to form the spacer-shaped floating gate on the dielectric spacer and over the gate dielectric layer.

7. The method of claim 1, wherein the step of forming the interlayer dielectric layer further comprises oxidizing a portion of the spacer-shaped floating gate by a thermal oxidation process.

8. The method of claim 1, wherein the step of forming the interlayer dielectric layer further comprises depositing the interlayer dielectric layer by a chemical vapor deposition process.

9. The method of claim 1, wherein the step of forming the control gate further comprises:

forming a polysilicon layer covering the substrate and filling the first opening;

forming a patterned photoresist layer on the polysilicon layer, wherein the patterned photoresist layer defines a control gate region;

etching the polysilicon layer to form the control gate by using the patterned photoresist layer as a mask; and

removing the patterned photoresist layer.

10. A method for forming a multi-bit stacked-type non-volatile memory array, comprising:

providing a silicon substrate;

forming a patterned arsenosilicate glass layer on the silicon substrate, wherein the patterned arsenosilicate glass layer defines a first opening, and the first opening exposes a portion of the silicon substrate and a plurality of side walls of the patterned arsenosilicate glass layer;

forming a plurality of silicon nitride spacers on the side walls of the patterned arsenosilicate glass layer;

forming a source/drain region in the silicon substrate;

forming a gate dielectric layer on the exposed portion of silicon substrate;

forming a plurality of spacer-shaped floating gates on the side walls of the silicon nitride spacers and over the gate dielectric layer;

forming an interlayer dielectric layer covering the spacer-shaped floating gates; and

forming a control gate covering the first opening.

11. The method of claim 10, wherein the step of forming the patterned arsenosilicate glass layer further comprises:

forming an arsenosilicate glass layer on the silicon substrate;

forming a patterned photoresist layer on the arsenosilicate glass layer, wherein the patterned photoresist layer defines the first opening;

etching the arsenosilicate glass layer to form the patterned arsenosilicate glass layer by using the patterned photoresist layer as a mask, wherein the portion of the silicon substrate and the side walls of the patterned arsenosilicate glass layer are exposed; and

removing the patterned photoresist layer.

12. The method of claim 10, wherein the step of forming the patterned arsenosilicate glass layer further comprises forming a plurality of arsenosilicate glass islands, and wherein two adjacent arsenosilicate glass islands define the first opening.

13. The method of claim 12, wherein the step of forming the source/drain region further comprises diffusing arsenic atoms of the arsenosilicate glass islands into the silicon substrate to form a bit line by a thermal driving process.

14. The method of claim 10, wherein the step of forming the silicon nitride spacers further comprises:

forming a conformal silicon nitride layer covering the silicon substrate; and

anisotropically etching the conformal silicon nitride layer to form the silicon nitride spacers on the side walls of the patterned arsenosilicate glass layer.

15. The method of claim 10, wherein the step of forming the source/drain region further comprises diffusing the arsenic atoms of the patterned arsenosilicate glass layer into the silicon substrate by thermal driving process.

16. The method of claim 10, wherein the step of forming the gate dielectric layer further comprises oxidizing the exposed silicon substrate to form the gate dielectric layer by thermal oxidation process.

17. The method of claim 10, wherein the step of forming the spacer-shaped floating gates further comprises:

forming a conformal polysilicon layer covering the silicon layer; and

anisotropically etching the conformal polysilicon layer to form the spacer-shaped floating gates on the silicon nitride spacers and over the gate dielectric layer.

18. The method of claim 10, wherein the step of forming the interlayer dielectric layer further comprises oxidizing a portion of the spacer-shaped floating gates by a thermal

oxidation process.

19. The method of claim 10, wherein the step of forming the interlayer dielectric layer further comprises depositing a dielectric layer by a chemical vapor deposition process.

20. The method of claim 10, wherein the step of forming the control gate further comprises:

forming a polysilicon layer covering the silicon substrate and filling the first opening;

forming a patterned photoresist layer on the polysilicon layer, wherein the patterned photoresist layer defines a control gate region;

etching the polysilicon layer to form a plurality of word lines by using the patterned photoresist layer as a mask; and

removing the patterned photoresist layer.

21. A structure of a multi-bit stacked-type non-volatile memory, comprising:

a substrate;

two dielectric islands containing arsenic on the substrate and defining an active area between the dielectric islands, wherein each of the dielectric islands includes a side wall;

two source/drain regions in the substrate being respectively located below two dielectric islands;

two dielectric spacers respectively disposed on two side walls of the dielectric islands;

a gate dielectric layer on the active area;

two spacer-shaped floating gates on the gate dielectric layer and being respectively located on two side walls of the dielectric spacers;

an interlayer dielectric layer on the spacer-shaped floating gates; and

a control gate filling the active area.